

WHAT IS CLAIMED IS:

1. A sigma delta converter comprising:
an integrator circuitry including an integrator input and an integrator output,
wherein an input signal coupled to the integrator input has an input AC
voltage component and a DC offset component;
a pair of capacitors coupled to the integrator input;
a first set of switches coupled the pair of capacitors, the first set of switches
configured to transfer a first charge to the pair of capacitors during a
first phase, the first charge proportional to a reference voltage; and
a second set of switches coupled to the pair of capacitors, the second set of
switches configured to transfer the first charge and a second charge to
the integrator input, the second charge proportional to the DC offset
component.
2. The sigma delta modulator, as recited in Claim 1, further comprising:
a comparator coupled to the integrator circuitry output, the comparator
including a comparator output.
3. The sigma delta modulator, as recited in Claim 1, wherein the integrator
circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta
loop filter, each of the N integrators having a first input, a second input, a first output
and a second output, each of the N integrators having a first integrator capacitor
coupled to the first input and the first output and a second integrator capacitor coupled
to the second input and the second output.

4. The sigma delta modulator, as recited in Claim 1, further comprising:
a comparator coupled to the integrator circuitry output, the comparator
including a comparator output;
a third set of switches coupled to the pair of capacitors, the third set of
switches configured to change a polarity of the first charge and the
second charge based on the comparator output; and
a fourth set of switches coupled to the pair of capacitors, the fourth set of
switches configured to change a polarity of the second charge based on
the comparator output, wherein the polarity of the second charge is
configured to cancel the DC offset component of the input signal.
5. The sigma delta modulator, as recited in Claim 1, further comprising:
a digital to analog converter coupled to the pair of capacitors for producing the
second charge.
6. The sigma delta modulator, as recited in Claim 5, the digital to analog
converter configured to receive a multi-bit code word input from a digital signal
processor.
7. The sigma delta modulator, as recited in Claim 1, wherein the integrator is
a continuous time integrator.
8. The sigma delta modulator, as recited in Claim 1, wherein the integrator is
a discrete time integrator.

9. A radio frequency (RF) signal receive path comprising:
 an intermediate frequency amplifier (IFA) including an IFA output;
 a plurality of anti-aliasing filters (AAFs) coupled to the IFA output, the AAFs
 having an AAF output; and
 a sigma delta modulator coupled to the AAF output, the sigma delta modulator
 comprising:
 integrator circuitry including an integrator input and an integrator
 output, wherein an input signal coupled to the integrator input
 has an input AC voltage component and a DC offset
 component;
 a pair of capacitors coupled to the integrator input;
 a first set of switches coupled the pair of capacitors, the first set of
 switches configured to transfer a first charge to the pair of
 capacitors during a first phase, the first charge proportional to a
 reference voltage; and
 a second set of switches coupled to the pair of capacitors, the second
 set of switches configured to transfer the first charge and a
 second charge to the integrator input, the second charge
 proportional to the DC offset component.

10. The RF signal receive path, as recited in Claim 9, wherein the integrator
 circuitry comprises N integrators coupled in series forming an Nth-Order sigma delta
 converter, each of the N integrators having a first input, a second input, a first output
 and a second output, each of the N integrators having a first integrator capacitor
 coupled to the first input and the first output and a second integrator capacitor coupled
 to the second input and the second output.

11. The RF signal receive path, as recited in Claim 9, the sigma delta modulator further comprising:
- a comparator coupled to the integrator output, the comparator including a comparator output;
 - a third set of switches coupled to the pair of capacitors, the third set of switches configured to change a polarity of the first charge and the second charge based on the comparator output; and
 - a fourth set of switches coupled to the pair of capacitors, the fourth set of switches configured to change a polarity of the second charge based on the comparator output, wherein the polarity of the second charge is configured to cancel the DC offset component of the input signal.
12. The RF signal receive path, as recited in Claim 9, the sigma delta modulator further comprising:
- a digital to analog converter coupled to the pair of capacitors for producing the second charge.
13. The RF signal receive path, as recited in Claim 12, the digital to analog converter configured to receive a multi-bit code word input from a digital signal processor.
14. The RF signal receive path, as recited in Claim 9, wherein the integrator is a continuous time integrator.
15. The RF signal receive path, as recited in Claim 9, wherein the integrator is a discrete time integrator.

16. A method comprising:
during a first phase, charging a pair of capacitors to a reference charge;
during a second phase, transferring a sum charge to inputs of a first integrator
in a series of integrators in a sigma delta modulator, the sum charge
including the reference charge and a DC offset correction charge.

17. The method, as recited in Claim 16, further comprising:
comparing an output of a last integrator in the series of integrators to a zero
value; and
determining a polarity of the reference charge in the sum charge based on a
result of the comparing.

18. The method, as recited in Claim 17, wherein a polarity of the DC offset
correction charge in the sum charge is independent of a result of the comparing.